A Programmable Multi-channel Sub-threshold FIR Filter for a Body Sensor Node

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***Abstract*—We propose a fully synthesizable, sub-threshold, multi-channel finite impulse response (FIR) filter for a batteryless body sensor network that employs energy harvesting. The filter can be programmed to use 15, 30, or 60 taps to tradeoff energy and accuracy depending on the available energy on chip. The filter uses a serial, resource-shared architecture that is replicated over four channels. A filter controller block is included to control data flow from the on-chip ADC to its respective filtering channel. Clock gating channels not in use as well as power gating the total block are used to save energy and reduce leakage. The proposed design is also highly programmable in terms of number of taps, number of active channels, number of simultaneous filters per data stream, and coefficient registers. The design was synthesized using standard cells in a 130nm commercial technology and consumes 118nW per channel when operating at 0.4V at 100kHz. For one channel, the filter has a lower energy and figure of merit (FOM) than current sub-threshold FIR filter designs.**

***Index Terms*—FIR, sub-threshold, biomedical signal processing, ECG, EEG, DSP**

I. Introduction

With the emergence of wireless sensor nodes and other energy-constrained systems with a relatively low throughput demand, low-power signal processing becomes crucial. For body sensor nodes that operate on harvested energy, operating in sub-threshold by reducing the supply voltage, V_{DD}, below the threshold voltage, V_T, can result in quadratic energy savings. Sub-threshold operation is well-suited for applications with reduced performance specifications due to circuits operating using leakage currents. For the body sensor node presented in [2] containing this design, the digital portion of the chip included a general purpose processor (GPP) and application specific accelerators all operated in the sub-threshold regime. This was completed while also meeting the specifications and throughput demands for processing ExG data. Filtering is a frequently used operation on chip but does not map well to a control-flow based block such as a GPP. Having a custom accelerator block for filtering allows for an order of magnitude less of power savings and cycle counts to achieve the same number of taps on the GPP as seen in [2].

For this chip, we used the filter for processing EEG/ECG signals to determine the amount of cortical neuronal activity in the brain [3]. This activity can be extracted from four key frequency bands: α (8-12Hz), β (18-26Hz), low-γ (30-50Hz), and γ (70-100Hz). Useful energy data can be extracted with sampling rates in the hundreds of Hz by Nyquist's. The presented FIR was designed considering these bands of interest, but is not limited to this application. Other sub-threshold filters have been proposed that use body-biasing techniques to reduce the effects of variation as in [4] or boost a sub-threshold supply voltage to the super-threshold region so that the circuit no longer operates in sub-threshold as in [5]. To maintain the portability of the design through the use of the synthesis flow, body-biasing was not used as it requires hand-layout. Similarly, over-driving devices to operate in linear mode while using a sub-threshold supply voltage was not considered a truly sub-threshold design. Prior work also used fewer than 15 taps and was not programmable, while the proposed filter can be programmed to use 15, 30, or 60 taps. This allows for a dynamic tradeoff between FIR energy and accuracy based on available energy on chip.

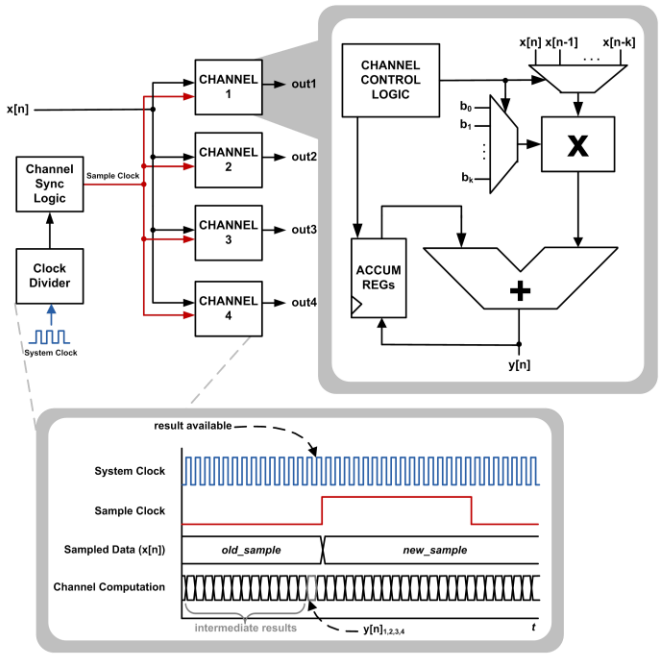

Fig. 1 Architecture of the 4-channel FIR including architecture of the channel. Timing diagram depicting operation of the serial architecture is included. A new result is available on every positive edge of the system clock before a new sample arrives on the positive edge of the sample clock.

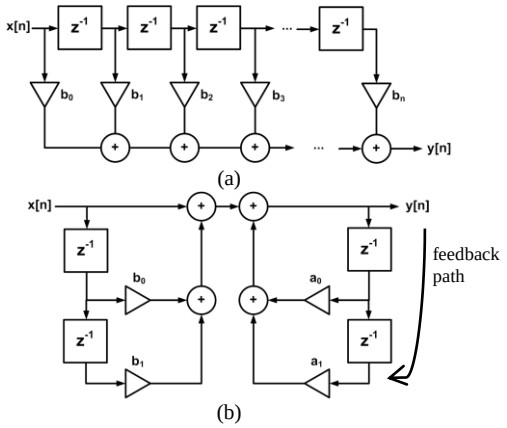

Fig. 2. FIR architecture and IIR architecture. (a) The direct-form FIR architecture. (b) The direct form IIR architecture showing feedback path.

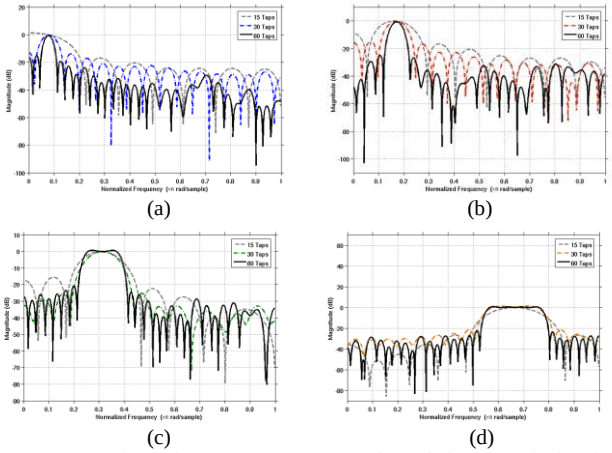

Fig. 3 Measured FIR frequency response for the α, β, low-γ, and γ bands for tap lengths of 15, 30, and 60.

II. Design Considerations

Prior to implementing the design using an FIR filter, an infinite-impulse response (IIR) architecture was considered, both architectures are seen in Fig. 2. IIR designs are desirable since they require fewer taps to achieve the same cutoff steepness as an FIR. Problems with IIR filters include the non-linear phase and the instability due to feedback. The non-linear phase was tolerable looking at the Bode plots for the bands of interest. To determine stability for the IIR passbands under consideration, the pole/zero plots were created using MATLAB's FDATool. Many of the pole locations fell very close to the unit circle, indicating a high possibility for instability. Quantization of the coefficients and data dependencies also had the potential to worsen this.

As stability could be an issue considering the specifications, the FIR implementation was the better option. The direct-form FIR architecture computes the result in parallel using as many adders and multipliers as there are taps. This would result in a much higher throughput than required for the design as well as a large area penalty for 30 taps replicated over four channels. A 200kHz crystal was available on chip for digital processing, while the sampling rate of the ExG signals was below 256Hz. Resource reuse of the arithmetic units was achieved through using the 200kHz clock for serially processing data between input samples [1]. This allows for a higher utilization of arithmetic units per sample resulting in lower leakage from inactive circuits. It also reduces the area penalty of a relatively large-tap design.

Since the filter is not always on the datapath on chip, it requires the block to have extremely low leakage when not in use. To further reduce leakage energy, appropriately sized PMOS headers were added to the design. When the block is not being used, the header will cut off the voltage supply to the gates reducing leakage due to its exponential dependence on V_{DS}. The filter can also be clock gated at the block or individual channel level. This prevents excess switching energy from being consumed due to an active system clock when the filter is not in use.

TABLE I
DESIGN SUMMARY

Technology	130nm 1.2V CMOS
Taps	15/30/60
Voltage Range	0.3V – 0.7V
Frequency Range	8kHz-6MHz
Area	0.23mm^2

III. FIR Design

A. Architecture and Channel Design

To extract accurate ExG data, a minimum of four leads is required. To process this data, the architecture of the FIR has four independent channels as seen in Fig. 1. Each channel is a replica of the other containing one 8-bit Baugh-Wooley multiplier, one 8-bit adder, coefficient registers, and a small amount of control logic. Each channel can be considered "real-time" processing since it can process one output sample for every input sample.

On the final chip, the sample clock was ~700x slower than that of the kHz range system clock used for digital processing. This allowed the architecture of each channel to be resource-shared and perform multiple tap computations per sampling period as shown in the timing diagram in Fig. 1. By sharing arithmetic units within each channel, the overall area was reduced. This way, the possible number of taps in the filter depended on the ratio of the system clock period to the sample clock period. As a 30 tap filter met the accuracy specifications for the design, each channel was individually clock-gated for the remaining ~600 clock cycles after the result had been computed. This also reduced the switching energy per sample. The number of filter taps was chosen based on analysis of the degradation point for the cutoff frequency and the passband attenuation for the EEG passbands.

The programmability allows for several operating modes that are decided at program time. In instances when accuracy is not critical but speed and power consumption are, a 15-tap mode is available. When accuracy is critical, a 60-tap mode can be created through the use of two channels and an adder on the chip's MCU, which is functionally equivalent as seen in (1). The use of the 60 tap mode requires the delay of 60

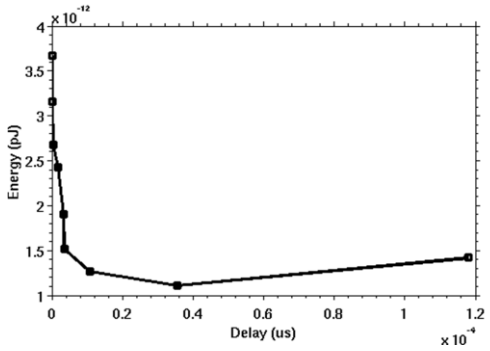

Fig. 4 Measured energy-delay curve for one active channel using 30 taps.

sample clock cycles plus the additional latency of one operation on the MCU.

$$y[n] = y[n]_{ch1} + y[n]_{ch2} = (b_0x[n] + b_1x[n-1] + \cdots + b_{29}x[n-29])_{ch1} + (b_{30}x[n-30] + (b_{31}x[n-31] + \cdots + b_{59}x[n-59])_{ch2} \quad (1)$$

Each channel of data can be programmed to be filtered using one FIR channel or two simultaneously with different filtering coefficients. Programmability is important with the volatility of energy on the capacitor while using energy harvesting. If energy dips below a certain level, fewer taps can be used to achieve the result with less accuracy. Trading off accuracy with energy also allows for processing different types of data with different fidelity requirements.

IV. Experimental Results

The filter was synthesized using only standard cells and fabricated in a commercial 130nm technology. It was tested to operate in the voltage range of 0.3V-0.7V with a corresponding frequency range of 8kHz-6MHz as seen in the design summary in Table I. Using PMOS headers allowed for leakage reduction when the block was not in the datapath. Clock gating channels during inactivity once the result had been computed also reduced switching energy. The frequency response of the FIR in the EEG/ECG energy extraction bands show that coefficient quantization had little effect on cutoff steepness, but caused distortion in the stopband ripple that is tolerable for the application as seen in Fig. 3. This figure also shows the accuracy benefits of going from the 15, 30, and 60 tap modes in the α, β, low-γ, and γ frequency bands. A measured energy-delay plot is shown in Fig. 4 with a minimum energy-delay point occurring at 350mV at 30kHz.

TABLE II
DESIGN COMPARISON

	This Work	[4]	[5]	[3]
Type	30-tap, 8-bit	8-tap, 8-bit	14-tap, 8-bit	4th order analog
Channels	4	1	1	4
Programmable	✓	×	×	×
Technology	0.13µm	0.13µm	0.13µm	0.13µm
Supply	0.4V	0.2V	0.27V	1.2V
Frequency	100kHz	12kHz	20MHz	20kHz
Power	118nW	114nW	310µW	780nW
Energy	1.18pJ	9.5pJ	15.57pJ	39pJ
FOM*	0.61	18.55	17.37	N/A

*FIR FOM: power(nW)/frequency(MHz)/# of taps/input bit length/coefficient bit length

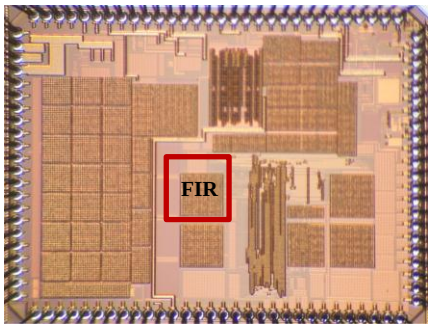

Fig. 5 Die photo of body sensor node including FIR filter.

The die photo annotated to show the FIR in relation the rest of the chip is shown in Fig. 5. Recent sub-threshold FIR filters have included fewer than 15 taps, consumed more energy, and have a higher FOM without the flexibility of this design as seen in Table II. The design operates down to 300mV at 8kHz, and measurements show that it consumes 118nW and 1.18pJ when one channel is active at 100kHz using 30 taps (frequency of filter when used on chip).

V. Conclusion

A programmable sub-threshold FIR filter was designed for use in low-throughput and ultra-low power designs such as body sensor networks. Although presented here for a single biomedical application, this filter is flexible enough for use in general purpose DSP applications. By serializing the traditional FIR architecture, the number of adders and multipliers required for the design was reduced, thereby reducing active and leakage energy for the overall design. As the filter was synthesized using only standard cells, the design is also highly portable for new technologies.

Acknowledgments

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